

CALL FOR PAPERS
Special Section on the 2009 International Symposium on Networks-on-Chip (NOCS)
in the
IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems

The IEEE Transactions on Computer-Aided design of Integrated Circuits and Systems (T-CAD) seeks original manuscripts for a Special Section on Networks-on-Chip (NoCs) scheduled to appear in the second half of 2010. Authors of papers that appeared at NOCS 2009 are invited to submit extended versions of their work to this issue.

Systems-on-Chip (SoCs) will soon contain hundreds of processing cores and IPs and so the focus of SoC architects is shifting from individual cores towards the design and optimization of the communication infrastructure. Consequently, on-chip and in-package, interconnect technology from circuits to network architectures, to interconnect design methodologies and CAD tools are all becoming critical and challenging factors for tomorrow high end SoCs.

This special section aims at exploring design methods and CAD tools for many-core on-chip and in-package interconnect networks at all levels of abstraction. In particular, topics of interest include but are not limited to:

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| <input type="checkbox"/> Network architecture (topology, routing, arbitration, etc.) | <input type="checkbox"/> NoC design methodologies and tools |
| <input type="checkbox"/> Network design for 3D stacked logic and memory | <input type="checkbox"/> Modeling, simulation and synthesis of NoCs |
| <input type="checkbox"/> Mapping of applications onto NoCs | <input type="checkbox"/> Quality of Service |
| <input type="checkbox"/> Power, energy, and reliability issues | <input type="checkbox"/> NoC support for CMP/MPSoCs |
| <input type="checkbox"/> Timing, synchronous/asynchronous communication | <input type="checkbox"/> Optical & RF for on-chip/in-package interconnects |
| <input type="checkbox"/> Programming models, memory support, cache access, etc. | <input type="checkbox"/> Signaling and circuit design for NoC links |
| <input type="checkbox"/> OS support for NoCs | <input type="checkbox"/> Floorplan-aware NoC optimization |
| <input type="checkbox"/> Metrics and benchmarks for NoCs | <input type="checkbox"/> NoC verification, debug & test |
| <input type="checkbox"/> Multi/many-core workload characterization & evaluation | <input type="checkbox"/> NoC case studies, NoC prototypes, etc. |

Submitted articles must not have been previously published or currently submitted for journal publication elsewhere. In accordance with TCAD policy, authors of NOCS 2009 papers should be aware that there should be a significant amount of additional technical material in the submitted journal paper. Authors are responsible for understanding and adhering to the TCAD submission guidelines, which can be accessed at <http://tcad.polito.it/authors.html>. Please thoroughly read these before submitting your manuscript.

Papers should be submitted to the TCAD submission site at <http://tcad.polito.it/Forms/Authors/index.html>. Authors should clearly identify their papers as submissions for this Special Section by using the prefix "NOCS09" before their paper title (e.g., "NOCS09: My Wonderful NOC Solution"). Feel free to contact the Guest Editors at radum@cmu.edu, or axel@kth.se, if you have questions. Note the following important dates.

Important dates:

Submission Deadline: September 15, 2009 Major Revision Due: December 11, 2009

Notification of Acceptance: January 25, 2010

Publication Materials for Final Manuscripts Due: February 12, 2010

Please address all other correspondence regarding this special section to Guest Editors **R. Marculescu** and **A. Jantsch**.

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